Freescale Semiconductor
Data Sheet: Advance Information
An Energy Efficient Solution by Freescale

Document Number: MAG3110
Rev 7, 10/2011

Three-Axis, Digital Magnetometer

MAG3110

Freescale's MAG3110 is a small, low-power, digital 3-axis magnetometer.

The device can be used in conjunction with a 3-axis accelerometer to produce orientation independent accurate compass heading information. It features a standard I^2C serial interface output and smart embedded functions.

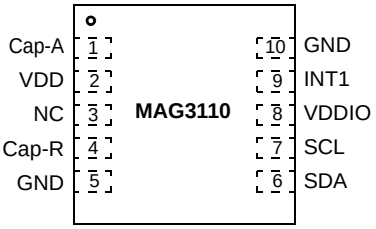
The MAG3110 is capable of measuring magnetic fields with an Output Data Rate (ODR) up to 80 Hz; these output data rates correspond to sample intervals from 12 ms to several seconds.

The MAG3110 is available in a plastic DFN package and it is guaranteed to operate over the extended temperature range of -40°C to +85°C.

Top and Bottom View

10-PIN DFN
2 mm by 2 mm by 0.85 mm
CASE 2154-01

Top View



Pin Connections

Features

- 1.95V to 3.6V Supply Voltage (VDD)
- 1.62V to VDD IO Voltage (VDDIO)
- Ultra Small 2 mm by 2 mm by 0.85 mm, 0.4 mm Pitch, 10-Pin Package
- Full Scale Range ±1000 μT
- Sensitivity of 0.10 μT
- Noise down to 0.25 μT rms
- Output Data Rates (ODR) up to 80 Hz
- I^2C digital output interface (operates up to 400 kHz Fast Mode)
- 7-bit I^2C address = 0x0E
- Sampled Low Power Mode
- RoHS compliant

Applications

- Electronic Compass
- Dead-reckoning assistance for GPS backup
- Location-based Services

ORDERING INFORMATION			
Part Number	**Temperature Range**	**Package Description**	**Shipping**
MAG3110FCR1	-40°C to +85°C	DFN-10	Tape and Reel (1000)
MAG3110FCR2	-40°C to +85°C	DFN-10	Tape and Reel (4000)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Application Notes for Reference

The following is a list of Freescale Application Notes written for the MAG3110:

- **AN4246**, *Calibrating an eCompass in the Presence of Hard and Soft Iron Interference*
- **AN4247**, *Layout Recommendations for PCBs using a Magnetometer Sensor*
- **AN4248**, *Implementing a Tilt-Compensated eCompass using Accelerometer and Magnetometer Sensors*
- **AN4249**, *Accuracy of Angle Estimation in eCompass and 3-D Pointer Applications*
- **AN1902**, *Quad Flat Pack No-Lead (QFN) Micro Dual Flat Pack No-Lead (μDFN)*

1 Block Diagram and Pin Description

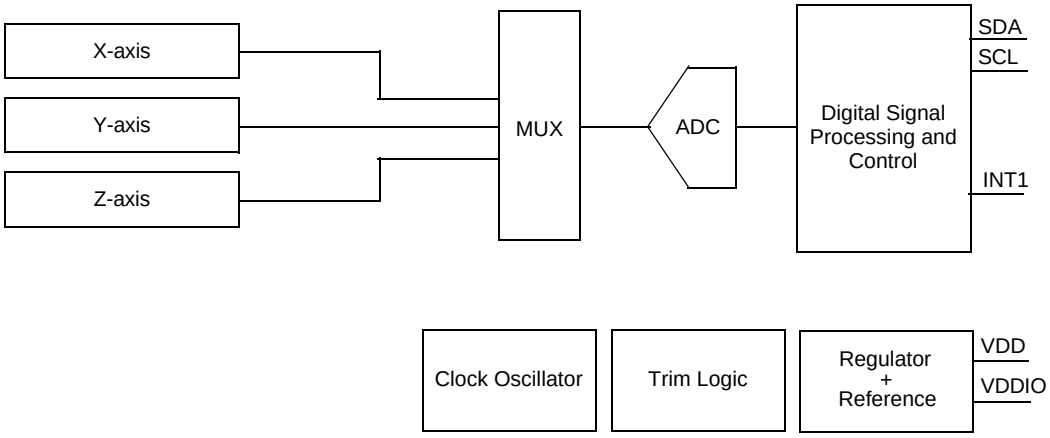


Figure 1. Block Diagram

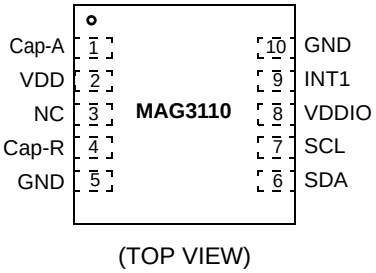


Figure 2. Pin Connections

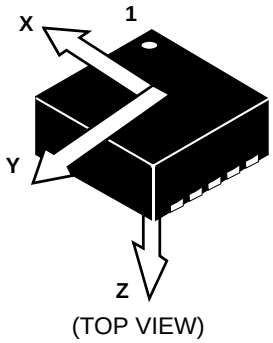


Figure 3. Measurement Coordinate System

Table 1. Pin Descriptions

Pin	Name	Function
1	Cap-A	Bypass Cap for Internal Regulator
2	VDD	Power Supply, 1.95V – 3.6V
3	NC	Do not connect.
4	Cap-R	Cap for Reset Pulse
5	GND	GND
6	SDA	I^2C Serial Data (Write = 0x1C; Read = 0x1D)
7	SCL	I^2C Serial Clock
8	VDDIO	Power for I/O Buffers, 1.65V - VDD
9	INT1	Interrupt - Active High Output
10	GND	GND

1.1 Application Circuit

The device power is supplied through VDD line. Power supply decoupling capacitors (100 nF ceramic) should be placed as near as possible to pins 1 and 2 of the device. VDDIO supplies power for the I/O pins SCL, SDA, and INT1.

The control signals SCL and SDA, are not tolerant of voltages more than VDDIO + 0.3 volts. If VDDIO is removed, the control signals SCL and SDA will clamp any logic signals with their internal ESD protection diodes.

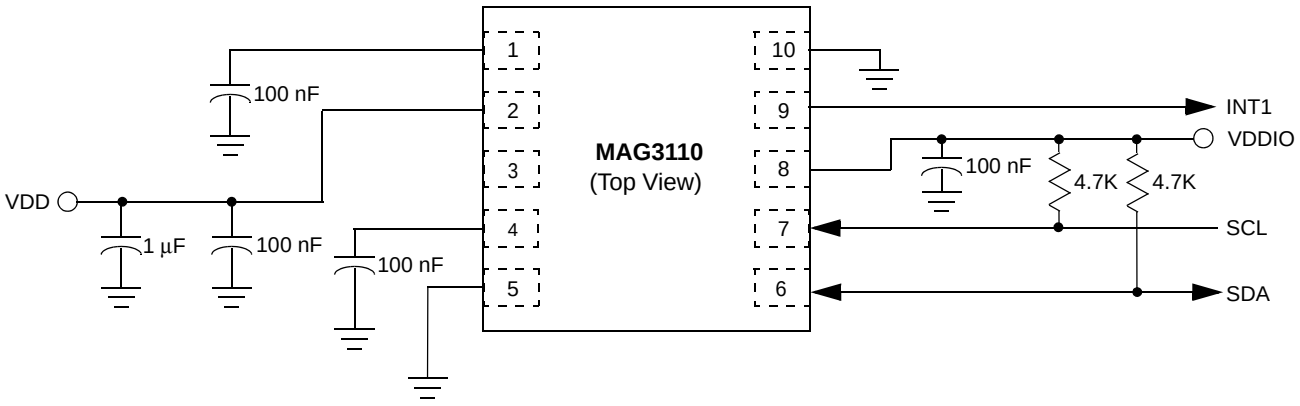


Figure 4. Electrical Connection

2 Operating and Electrical Specifications

2.1 Operating Characteristics

Table 2. Operating Characteristics @ VDD = 1.8 V, T = 25°C unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Full Scale Range		FS		±1000		µT
Output Data Range (CTRL_REG2[RAW] = 1)			-20,000		20,000	bits
Output Data Range (CTRL_REG2[RAW] = 0)(1)			-30,000		30,000	bits
Sensitivity		So		0.10		µT/bit
Sensitivity Change vs. Temperature		Tcs		±0.1		%/°C
Zero Flux Offset Accuracy				±1000		µT
Hysteresis(2)				0.25	1	%
Non Linearity Best Fit Straight Line(3)		NL	-1	±0.3	1	%FS
Magnetometer Output Noise	OS = 00(4)	Noise		0.4		µT rms
	OS = 01			0.35		
	OS = 10			0.3		
	OS = 11			0.25		
Operating Temperature Range		T_{op}	-40		+85	°C

1. Maximum user defined offset must be within ±10,000 counts.
2. Hysteresis is from 0 µT to 1000 µT to 0 µT and from 0 µT to -1000 µT to 0 µT.
3. Best Fit Straight Line 0 to ±1000 µT.
4. OS = Over Sampling Ratio.

2.2 Absolute Maximum Ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	VDD	-0.3 to +3.6	V
Input Voltage on any Control Pin (SCL, SDA)	Vin	-0.3 to VDDIO + 0.3	V
Maximum Applied Magnetic Field	—	100,000	µT
Operating Temperature Range	T_{op}	-40 to +85	°C
Storage Temperature Range	T_{STG}	-40 to +125	°C

Table 4. ESD and Latchup Protection Characteristics

Rating	Symbol	Value	Unit
Human Body Model	HBM	±2000	V
Machine Model	MM	±200	V
Charge Device Model	CDM	±500	V
Latchup Current at T = 85°C	—	±100	mA

This device is sensitive to mechanical shock. Improper handling can cause permanent damage of the part or cause the part to otherwise fail.

This device is sensitive to ESD, improper handling can cause permanent damage to the part.

2.3 Electrical Characteristics

Table 5. Electrical Characteristics @ VDD = 2.0V, VDDIO = 1.8V, T = 25°C unless otherwise noted

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Supply Voltage		VDD	1.95	2.4	3.6	V
Interface Supply Voltage		VDDIO	1.62		VDD	V
Supply Current in ACTIVE Mode	ODR[1][2] 80 Hz, OS[1] = 00	I_{dd}		900		µA
	ODR 40 Hz, OS[3] = 00			550		
	ODR 20 Hz, OS[3] = 00			275		
	ODR 10 Hz, OS[3] = 00			137.5		
	ODR 5 Hz, OS[3] = 00			68.8		
	ODR 2.5 Hz, OS[3] = 00			34.4		
	ODR 1.25 Hz, OS[3] = 00			17.2		
	ODR 0.63 Hz, OS = 00			8.6		
Supply Current Drain in STANDBY Mode	Measurement mode off	I_{dd}Stby		2		µA
Digital High Level Input Voltage SCL, SDA		VIH	0.75*VDDIO			V
Digital Low Level Input Voltage SCL, SDA		VIL			0.3* VDDIO	V
High Level Output Voltage INT1	I_O = 500 µA	VOH	0.9*VDDIO			V
Low Level Output Voltage INT1	I_O = 500 µA	VOL			0.1* VDDIO	V
Low Level Output Voltage SDA	I_O = 500 µA	VOLS			0.1* VDDIO	V
Output Data Rate (ODR)		ODR	0.8*ODR	ODR	1.2 *ODR	Hz
Signal Bandwidth		BW			ODR/2	Hz
Boot Time from Power applied to Boot Complete		BT			10	ms
Turn-on Time[4][5]	OS = 1	T_{on}		25		ms
Operating Temperature Range		T_{op}	-40		+85	°C

1. ODR = Output Data Rate; OS = Over Sampling Ratio.
2. Please see Table 30 for all ODR and OSR setting combinations, as well as corresponding current consumption and noise levels.
3. By design.
4. Time to obtain valid data from STANDBY mode to ACTIVE Mode.
5. In 80 Hz mode ODR.

2.4 I²C Interface Characteristics

Table 6. I²C Slave Timing Values(1)

Parameter	Symbol	I²C Fast Mode		Unit
		Min	Max	
SCL Clock Frequency Pullup = 1 kΩ, C_b = 20 pF	f_{SCL}	0	400	kHz
Bus Free Time between STOP and START Condition	t_{BUF}	1.3		µs
Repeated START Hold Time	$t_{HD;STA}$	0.6		µs
Repeated START Setup Time	$t_{SU;STA}$	0.6		µs
STOP Condition Setup Time	$t_{SU;STO}$	0.6		µs
SDA Data Hold Time(2)	$t_{HD;DAT}$	0.05(3)	(4)	µs
SDA Valid Time (5)	$t_{VD;DAT}$		0.9(4)	µs
SDA Valid Acknowledge Time (6)	$t_{VD;ACK}$		0.9(4)	µs
SDA Setup Time	$t_{SU;DAT}$	100(7)		ns
SCL Clock Low Time	t_{LOW}	1.3		µs
SCL Clock High Time	t_{HIGH}	0.6		µs
SDA and SCL Rise Time	t_r	20 + 0.1C_b(8)	1000	ns
SDA and SCL Fall Time (3) (8) (9) (10)	t_f	20 + 0.1C_b(8)	300	ns
Pulse width of spikes on SDA and SCL that must be suppressed by input filter	t_{SP}		50	ns

1. All values referred to VIH (min) and VIL (max) levels.
2. $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
3. A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the VIH (min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
4. The maximum $t_{HD;DAT}$ could be must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This device does not stretch the LOW period (t_{LOW}) of the SCL signal.
5. $t_{VD;DAT}$ = time for Data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
6. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
7. A Fast mode I²C device can be used in a Standard mode I²C system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r(max) + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I²C specification) before the SCL line is released. Also the acknowledge timing must meet this setup time
8. C_b = total capacitance of one bus line in pF.
9. The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
10. In Fast mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

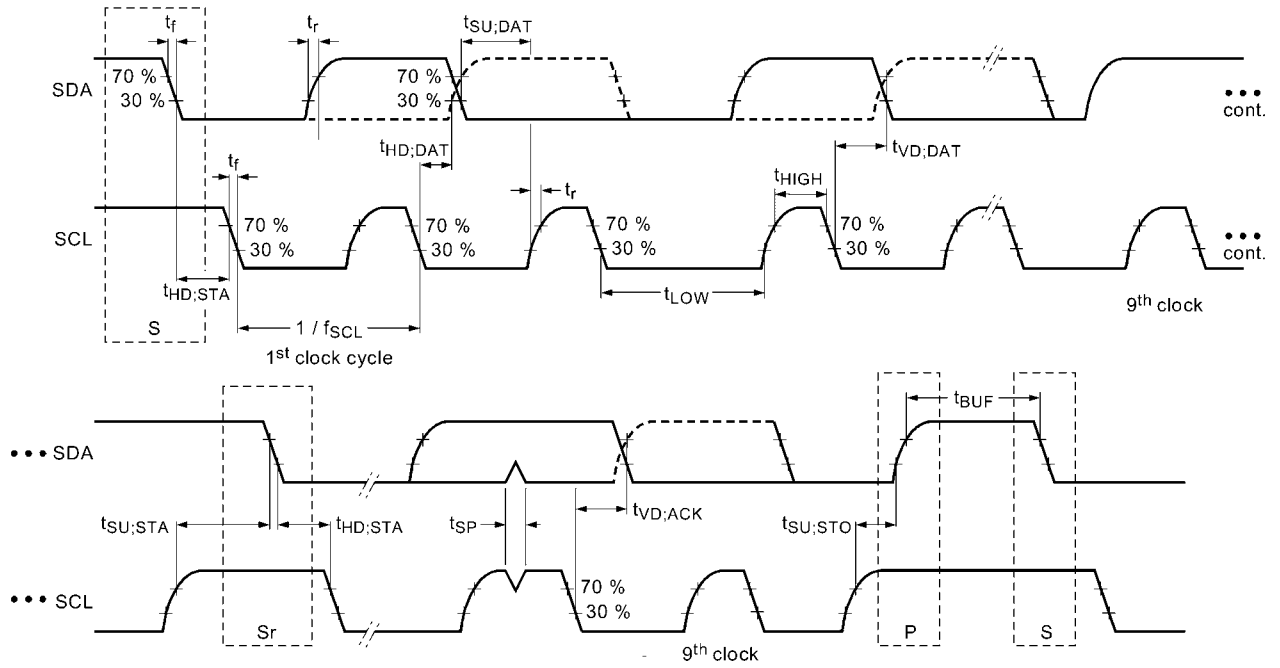


Figure 5. I²C Slave Timing Diagram

2.5 General I²C Information

The SCL and SDA signals are driven by open-drain buffers and a pullup resistor is required to make the signals rise to the high state. The value of the pullup resistors depends on the system I²C clock rate and the capacitance load on the I²C bus.

Higher resistance value pullup resistors consume less power, but have a slower the rise time (due to the RC time constant between the bus capacitance and the pullup resistor) and will limit the I²C clock frequency.

Lower resistance value pullup resistors consume more power, but enable higher I²C clock operating frequencies.

High bus capacitance is due to long bus lines or a high number of I²C devices connected to the bus. A lower value resistance pullup resistor is required in higher bus capacitance systems.

For standard 100 kHz clock I²C, pullup resistors typically are between 5k and 10 kΩ. For a heavily loaded bus, the pullup resistor value may need to be reduced. For higher speed 400 kHz or 800 kHz clock I²C, bus capacitance will need to be kept low, in addition to selecting a lower value resistance pullup resistor. Pullup resistors for high speed buses typically are about 1 KΩ.

In a well designed system with a microprocessor and one I²C device on the bus, with good board layout and routing, the I²C bus capacitance can be kept under 20 pF. With a 1K pullup resistor, the I²C clock rates can be well in excess of a few megahertz.

3 Modes of Operation

Table 7. Modes of Operation Description

Mode	I²C Bus State	Function Description
STANDBY	I²C communication is possible.	Only POR and digital blocks are enabled. Analog subsystem is disabled.
ACTIVE	I²C communication is possible.	All blocks are enabled (POR, Digital, Analog).

4 Functionality

MAG3110 is a small low-power, digital output, 3-axis linear magnetometer packaged in a 10-pin DFN. The device contains a magnetic transducer for sensing and an ASIC for control and digital I^2C communications.

4.1 I^2C Serial Interface

Communication with the MAG3110 takes place over an I^2C bus. The MAG3110 also has an interrupt signal indicating that new magnetic data readings are available. Interrupt driven sampling allows operation without the overhead of software polling.

4.2 Factory Calibration

MAG3110 is factory calibrated for sensitivity and temperature coefficient. All factory calibration coefficients are applied automatically by the MAG3110 ASIC before the magnetic field readings are written to registers 0x01 to 0x06 (see section 5). There is no need for the user to apply the calibration correction in the software and the calibration coefficients are not therefore accessible to the user.

The offset registers in the addresses 0x09 to 0x0E are not a factory calibration offset but allow the user to define a hard iron offset which can be automatically subtracted from the magnetic field readings (see section 4.3.4).

4.3 Digital Interface

Table 8. Serial Interface Pin Description

Pin Name	Pin Description
VDDIO	IO voltage
SCL	I^2C Serial Clock
SDA	I^2C Serial Data
INT	Data ready interrupt pin

There are two signals associated with the I^2C bus: the Serial Clock Line (SCL) and the Serial Data line (SDA). External pullup resistors (connected to VDDIO) are needed for SDA and SCL. When the bus is free, both lines are high. The I^2C interface is compliant with Fast mode (400 kHz), and Normal mode (100 kHz) I^2C standards.

4.3.1 General I^2C Operation

There are two signals associated with the I^2C bus: the Serial Clock Line (SCL) and the Serial Data Line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. External pullup resistors (connected to VDDIO) are expected for SDA and SCL. When the bus is free, both lines are high. The I^2C interface is compliant with fast mode (400 kHz), and normal mode (100 kHz) I^2C standards.

The transaction on the bus is started through a start condition (START) signal. START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After START has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after START contains the slave address in the first 7 bits, and the eighth bit, the read/write bit, indicates whether the Master is receiving data from the slave or transmitting data to the save. When an address is sent, each device in the system compares the first seven bits after a START condition with its own address. If they match, the device considers itself addressed by the Master. The 9th clock pulse, following the slave address byte (and each subsequent byte) is the acknowledge (ACK). The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock period.

The number of bytes per transfer is unlimited. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. This delay action is called clock stretching. Not all receiver devices support clock stretching. Not all masters recognize clock stretching.

This part does use clock stretching.

A low to high transition on the SDA line while the SCL line the SCL line is high is defined as a stop condition (STOP). A write or burst write is always terminated by the Master issuing a STOP. A Master should properly terminate a read by not acknowledging a byte at the appropriate time in the protocol. A Master may issue a repeated START during a transfer.

The MAG3110 I^2C 7-bit device address is 0x0E. In I^2C practice, the device address is shifted left by one bit field and a read/write bit is set in the lowest bit position. The I^2C 8-bit write address is therefore 0x1C and the read address 0x1D.

See Figure 6 for details on how to perform read/write operations with MAG3110.

Single/Burst Write Operation

I^2C Start	I^2C Slave ADDR (R/W bit = 0)	MAG3110 Register Address to Start Write	Data0*	Data1	—	I^2C STOP

* Data Bytes Outgoing

Single/Burst Read Operation

I^2C Start	I^2C Slave ADDR (R/W bit = 0)	MAG3110 Register Address to Start Read	I^2C Repeated Start	I^2C Slave ADDR (R/W bit = 1)	Data0*	Data1	—	I^2C STOP

* Data Bytes Incoming

Figure 6. MAG3110 I^2C Generic Read/Write Operations

4.3.2 Pullup

The SCL and SDA signals are driven by open-drain buffers and a pullup resistor is required to make the signals rise to the high state. The value of the pullup resistors depends on the system I^2C clock rate and the capacitance load on the I^2C bus.

Higher resistance value pullup resistors consume less power, but have a slower the rise time (due to the RC time constant between the bus capacitance and the pullup resistor) and will limit the I^2C clock frequency.

Lower resistance value pullup resistors consume more power, but enable higher I^2C clock operating frequencies.

High bus capacitance is due to long bus lines or a high number of I^2C devices connected to the bus. A lower value resistance pullup resistor is required in higher bus capacitance systems.

For standard 100 kHz clock I^2C, pullup resistors typically are between 5k and 10 kΩ. For a heavily loaded bus, the pullup resistor value may need to be reduced. For higher speed 400 kHz or 800 kHz clock I^2C, bus capacitance will need to be kept low, in addition to selecting a lower value resistance pullup resistor. Pullup resistors for high speed buses typically are about 1 KΩ.

In a well designed system with a microprocessor and one I^2C device on the bus, with good board layout and routing, the I^2C bus capacitance can be kept under 20 pF. With a 1K pullup resistor, the I^2C clock rates can be well in excess of a few megahertz.

4.3.3 Fast Read Mode

When the Fast Read (FR) bit is set (CTRL_REG1, 0x10, bit 2), the MSB 8-bit data is read through the I^2C bus. Auto-increment is set to skip over the LSB data. When FR bit is cleared, the complete 16-bit data is read accessing all 6 bytes sequentially (OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, OUT_Z_LSB).

4.3.4 User Offset Corrections

The 2's complement user offset correction register values are used to compensate for correcting the X, Y, and Z-axis after device board mount. These values may be used to compensate for hard iron interference.

Depending on the setting of the CTRL_REG2[RAW] bit, the magnetic field sample data is corrected with the user offset values (CTRL_REG2[RAW] = 0), or can be read out uncorrected for user offset values (CTRL_REG2[RAW] = 1). The factory calibration correction is always applied irrespective of the setting of the CTRL_REG2[RAW] bit. In order to not saturate the sensor output, offset values should be within ±10,000 counts.

The factory calibration for gain, offset and temperature compensation is always automatically applied irrespective of the setting of the CTRL_REG2[RAW] bit which only controls the subtraction of the user defined hard iron offset.

4.3.5 INT1

The DR_STATUS register (see section 5.1.1) contains the ZYXDR bit which denotes the presence of new measurement data on one or more axes. Software polling can be used to detect the transition of the ZYXDR bit from 0 to 1 but, since the ZYXDR bit is also logically connected to the INT1 pin, a more efficient approach is to use INT1 to trigger a software interrupt when new measurement data is available as follows:

1. Enable automatic resets by setting AUTO_MRST_EN bit in CTRL_REG2 (CTRL_REG2 = 0b1XXXXXX).
2. Put MAG3110 in ACTIVE mode (CTRL_REG1 = 0bXXXXXX01).
3. Idle until INT1 goes HIGH and activates an interrupt service routine in the user software.
4. Read magnetometer data as required from registers 0x01 to 0x06. INT1 is cleared when register 0x01 OUT_X_MSB is read and this register must therefore always be read in the interrupt service routine.
5. Return to idle in step 2.

4.3.6 Triggered Measurements

Set the TM bit in CTRL_REG1 when you want the part to acquire only 1 sample on each axis. See table below for details.

AC	TM	Description
0	0	ASIC is in low power standby mode.
0	1	The ASIC shall exit standby mode, perform one measurement cycle based on the programmed ODR and OSR setting, update the I^2C data registers and re-enter standby mode.
1	0	The ASIC shall perform continuous measurements based on the current OSR and ODR settings.
1	1	The ASIC shall continue current measurement at fastest applicable ODR for programmed OSR. The ASIC shall return to programmed ODR after completing the triggered measurement.

The anti-aliasing filter in the A/D converter has a finite delay before the output “settles”. The output data for the first ODR period after getting out of Standby mode is expected to be slightly off. This effect will be more pronounced for the lower over-sampling settings since with higher settings the error of the first acquisition will be averaged over the total number of samples. Therefore, it is not recommended to use TRIGGER MODE (CTRL_REG1[AC]=0, CTRL_REG1[TM]=1) measurements for applications that require high accuracy, especially in low OS settings.

4.3.7 MAG3110 Setup Examples

Continuous Measurements with ODR = 80 Hz, OSR = 1

1. Enable automatic resets by setting bit AUTO_MRST_EN in CTRL_REG2. (CTRL_REG2 = 0x80)
2. Put MAG3110 in active mode 80 Hz with OSR = 1 by writing 0x01 to CTRL_REG1 (CTRL_REG1 = 0x01)
3. At this point it is possible to sync with MAG3110 utilizing INT1 pin or using polling of the DR_STATUS register as explained in section 4.3.5.

Continuous Measurements with ODR = 0.63 Hz, OSR = 2

1. Enable automatic resets by setting bit AUTO_MRST_EN in CTRL_REG2. (CTRL_REG2 = 0x80)
2. Put MAG3110 in active mode 0.63 Hz with OSR = 2 by writing 0xC9 to CTRL_REG1 (CTRL_REG1 = 0xC9)
3. At this point, it is possible to sync with MAG3110 utilizing INT1 pin or using polling of the DR_STATUS register as explained in section 4.3.5.

Triggered Measurements with ODR = 10 Hz, OSR = 8

1. Enable automatic resets by setting bit AUTO_MRST_EN in CTRL_REG2. (CTRL_REG2 = 0x80)
2. Initiate a triggered measurement by writing 0b00011010 to CTRL_REG1 (CTRL_REG1 = 0b00011010).
3. MAG3110 will acquire the triggered measurement and go back into STANDBY mode. It is possible at this point to sync on INT1 or resort to polling of DR_STATUS register to read acquired data out of MAG3110.
4. Go to step 2 based on application needs.

5 Register Descriptions

Table 9. Register Address Map

Name	Type	Register Address	Auto-Increment Address (Fast Read)(1)	Default Value	Comment
DR_STATUS(2)	R	0x00	0x01	0000 0000	Data ready status per axis
OUT_X_MSB(2)	R	0x01	0x02 (0x03)	data	Bits [15:8] of X measurement
OUT_X_LSB(2)	R	0x02	0x03	data	Bits [7:0] of X measurement
OUT_Y_MSB(2)	R	0x03	0x04 (0x05)	data	Bits [15:8] of Y measurement
OUT_Y_LSB(2)	R	0x04	0x05	data	Bits [7:0] of Y measurement
OUT_Z_MSB(2)	R	0x05	0x06 (0x07)	data	Bits [15:8] of Z measurement
OUT_Z_LSB(2)	R	0x06	0x07	data	Bits [7:0] of Z measurement
WHO_AM_I(2)	R	0x07	0x08	0xC4	Device ID Number
SYSMOD(2)	R	0x08	0x09	data	Current System Mode
OFF_X_MSB	R/W	0X09	0x0A	0000 0000	Bits [14:7] of user X offset
OFF_X_LSB	R/W	0X0A	0X0B	0000 0000	Bits [6:0] of user X offset
OFF_Y_MSB	R/W	0X0B	0X0C	0000 0000	Bits [14:7] of user Y offset
OFF_Y_LSB	R/W	0X0C	0X0D	0000 0000	Bits [6:0] of user Y offset
OFF_Z_MSB	R/W	0X0D	0X0E	0000 0000	Bits [14:7] of user Z offset
OFF_Z_LSB	R/W	0X0E	0X0F	0000 0000	Bits [6:0] of user Z offset
DIE_TEMP(2)	R	0X0F	0X10	data	Temperature, signed 8 bits in °C
CTRL_REG1(3)	R/W	0X10	0X11	0000 0000	Operation modes
CTRL_REG2(3)	R/W	0X11	0x12	0000 0000	Operation modes

1. Fast Read mode for quickly reading the Most Significant Bytes (MSB) of the sampled data.
2. Register contents are preserved when transitioning from “ACTIVE” to “STANDBY” mode.
3. Modification of this register’s contents can only occur when device is “STANDBY” mode, except the TM and AC bit fields in CTRL_REG1 register.

5.1 Sensor Status

5.1.1 DR_STATUS (0x00)

Data Ready Status

This read-only status register provides the acquisition status information on a per-sample basis, and reflects real-time updates to the OUT_X, OUT_Y, and OUT_Z registers.

Table 10. DR_STATUS Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZYXOW	ZOW	YOW	XOW	ZYXDR	ZDR	YDR	XDR

Table 11. DR_STATUS Descriptions

ZYXOW	X, Y, Z-axis Data Overwrite. Default value: 0. 0: No data overwrite has occurred. 1: Previous X or Y or Z data was overwritten by new X or Y or Z data before it was completely read.
ZOW	Z-axis Data Overwrite. Default value: 0. 0: No data overwrite has occurred. 1: Previous Z-axis data was overwritten by new Z-axis data before it was read.
YOW	Y-axis Data Overwrite. Default value: 0. 0: No data overwrite has occurred. 1: Previous Y-axis data was overwritten by new Y-axis data before it was read.
XOW	X-axis Data Overwrite. Default value: 0 0: No data overwrite has occurred. 1: Previous X-axis data was overwritten by new X-axis data before it was read.
ZYXDR	X or Y or Z-axis new Data Ready. Default value: 0. 0: No new set of data ready. 1: New set of data is ready.
ZDR	Z-axis new Data Available. Default value: 0. 0: No new Z-axis data is ready. 1: New Z-axis data is ready.
YDR	Z-axis new Data Available. Default value: 0. 0: No new Y-axis data is ready. 1: New Y-axis data is ready.
XDR	Z-axis new Data Available. Default value: 0. 0: No new X-axis data is ready. 1: New X-axis data is ready.

ZYXOW is set to 1 whenever new data is acquired before completing the retrieval of the previous set. This event occurs when the content of at least one data register (i.e. OUT_X, OUT_Y, OUT_Z) has been overwritten. ZYXOW is cleared when the high-bytes of the data (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) of all active channels are read.

ZOW is set to 1 whenever new Z-axis acquisition is completed before the retrieval of the previous data. When this occurs the previous data is overwritten. ZOW is cleared any time OUT_Z_MSB register is read.

YOW is set to 1 whenever new Y-axis acquisition is completed before the retrieval of the previous data. When this occurs the previous data is overwritten. YOW is cleared any time OUT_Y_MSB register is read.

XOW is set to 1 whenever new X-axis acquisition is completed before the retrieval of the previous data. When this occurs the previous data is overwritten. XOW is cleared any time OUT_X_MSB register is read.

ZYXDR signals that new acquisition for any of the enabled channels is available. ZYXDR is cleared when the high-bytes of the data (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) of all the enabled channels are read.

ZDR is set to 1 whenever new Z-axis data acquisition is completed. ZDR is cleared any time OUT_Z_MSB register is read.

YDR is set to 1 whenever new Y-axis data acquisition is completed. YDR is cleared any time OUT_Y_MSB register is read.

XDR is set to 1 whenever new X-axis data acquisition is completed. XDR is cleared any time OUT_X_MSB register is read.

5.1.2 OUT_X_MSB (0x01), OUT_X_LSB (0x02), OUT_Y_MSB (0x03), OUT_Y_LSB (0x04), OUT_Z_MSB (0x05), OUT_Z_LSB (0x06)

X-axis, Y-axis, and Z-axis 16-bit output sample data of the magnetic field strength expressed as signed 2's complement numbers.

When RAW bit is set (CTRL_REG2[RAW] = 1), the output range is between -20,000 to 20,000 bit counts (the combination of the 1000 μT full scale range and the zero flux offset ranging up to 1000 μT).

When RAW bit is clear (CTRL_REG2[RAW] = 0), the output range is between -30,000 to 30,000 bit counts when the user offset ranging between -10,000 to 10,000 bit counts are included

The DR_STATUS register, OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, and OUT_Z_LSB are stored in the auto-incrementing address range of 0x00 to 0x06. Data acquisition is a sequential read of 6 bytes.

If the Fast Read (FR) bit is set in CTRL_REG1 (0x10), auto-increment will skip over LSB of the X, Y, Z sample registers. This will shorten the data acquisition from 6 bytes to 3 bytes. If the LSB registers are directly addressed, the LSB information can still be read regardless of FR bit setting.

The preferred method for reading data registers is the burst read method where the user application acquires data sequentially starting from register 0x01. If register 0x01 is not read, the rest of the data registers (0x02 - 0x06) will not be updated with the most recent acquisition. It is still possible to address individual data registers, however register 0x01 must be read prior to ensure reading latest acquisition.

Table 12. OUT_X_MSB Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XD15	XD14	XD13	XD12	XD11	XD10	XD9	XD8

Table 13. OUT_X_LSB Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0

Table 14. OUT_Y_MSB Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
YD15	YD14	YD13	YD12	YD11	YD10	YD9	YD8

Table 15. OUT_Y_LSB Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0

Table 16. OUT_Z_MSB Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZD15	ZD14	ZD13	ZD12	ZD11	ZD10	ZD9	ZD8

Table 17. OUT_Z_LSB Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZD6	ZD6	ZD5	ZD4	ZD3	ZD2	ZD1	ZD0

5.2 Device ID

5.2.1 WHO_AM_I (0x07)

Device identification register. This read-only register contains the device identifier which is set to 0xC4. This value is factory programmed. Consult factory for custom alternate values.

Table 18. WHO_AM_I Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	0	0	0	1	0	0

5.2.2 SYSMOD (0x08)

The read-only system mode register indicates the current device operating mode.

Table 19. SYSMOD Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	SYSMOD1	SYSMOD0

Table 20. SYSMOD Description

SYSMOD	System Mode. Default value: 00. 00: STANDBY mode. 01: ACTIVE mode, RAW data. 10: ACTIVE mode, non-RAW user-corrected data.

5.3 User Offset Correction

5.3.1 OFF_X_MSB (0x09), OFF_X_LSB (0x0A), OFF_Y_MSB (0x0B), OFF_Y_LSB (0x0C), OFF_Z_MSB (0x0D), OFF_Z_LSB (0x0E)

X-axis, Y-axis, and Z-axis user defined offsets in 2's complement format which are used when CTRL_REG2[RAW] = 0 (see section 5.5.2) to correct for the MAG3110 zero flux offset and for hard iron offsets on the PCB caused by external components. The maximum sensible range for the user offsets is in the range -10,000 to 10,000 bit counts comprising the sum of the correction for the zero flux offset (range -1000 μT to 1000 μT or -10,000 to 10,000 bit counts) and the PCB hard iron offset (range -1000 μT to 1000 μT or
-10,000 to 10,000 bit counts).

The user offsets are automatically subtracted by the MAG3110 logic when CTRL_REG2[RAW] = 0 before the magnetic field readings are written to the data measurement registers 0x01 to 0x06. The maximum range of the X, Y and Z data measurement registers when CTRL_REG2[RAW] = 0 is therefore -30,000 to 30,000 bit counts and is computed without clipping. The user offsets are not subtracted when CTRL_REG2[RAW] = 1. The least significant bit of the user defined X, Y and Z offsets is forced to be zero irrespective of the value written by the user.

If the MAG3110 zero flux offset and PCB hard iron offset corrections are performed by an external microprocessor (the most likely scenario) then the user offset registers can be ignored and the CTRL_REG2[RAW] bit should be set to 1.

The user offset registers should not be confused with the factory calibration corrections which are not user accessible and which are always applied to the measured magnetic data.

Table 21. OFF_X_MSB Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XD14	XD13	XD12	XD11	XD10	XD9	XD8	XD7

Table 22. OFF_X_LSB Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XD6	XD5	XD4	XD3	XD2	XD1	XD0	0

Table 23. OFF_Y_MSB Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
YD14	YD13	YD12	YD11	YD10	YD9	YD8	YD7

Table 24. OFF_Y_LSB Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
YD6	YD5	YD4	YD3	YD2	YD1	YD0	0

Table 25. OFF_Z_MSB Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZD14	ZD13	ZD12	ZD11	ZD10	ZD9	ZD8	ZD7

Table 26. OFF_Z_LSB Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZD6	ZD5	ZD4	ZD3	ZD2	ZD1	ZD0	0

5.4 Temperature

5.4.1 DIE_TEMP (0x0F)

Temperature °C expressed as an 8-bit 2's complement number, however, the temperature is not trimmed for offset and the compensation for offset must be done in user application. The sensitivity of the temperature reading is correct. **Note:** The register allows for temperatures from -128°C to 127°C but the output range is from -40°C to 125°C.

Table 27. TEMP Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T7	T6	T5	T4	T3	T2	T1	T0

5.5 Control Registers

5.5.1 CTRL_REG1 (0x10)

Note: Except for STANDBY mode selection (Bit 0, AC), the device must be in STANDBY mode to change any of the fields within CTRL_REG1 (0x10).

Table 28. CTRL_REG1 Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DR2	DR1	DR0	OS1	OS0	FR	TM	AC

Table 29. CTRL_REG1 Description

DR[2:0]	Data rate selection. Default value: 000. See Table 30 for more information.
OS [1:0]	This register configures the over sampling ratio or measurement integration time. Default value: 00. See Table 30 for more information.
FR	Fast Read selection. Default value: 0. 0: The full 16-bit values are read. 1: Fast Read, 8-bit values read from the MSB registers.
TM	Trigger immediate measurement. Default value: 0 0: Normal operation based on AC condition. 1: Trigger measurement. If part is in ACTIVE mode, any measurement in progress will continue with the highest ODR possible for the selected OSR. In STANDBY mode triggered measurement will occur immediately and part will return to STANDBY mode as soon as the measurement is complete.
AC	Operating mode selection. **Note:** see section 4.3.6 for details. Default value: 0. 0: STANDBY mode. 1: ACTIVE mode. ACTIVE mode will make periodic measurements based on values programmed in the Data Rate (DR) and Over Sampling Ratio bits (OS).

Table 30. Over Sampling Ratio and Data Rate Description

DR2	DR1	DR0	OS1	OS0	Output Rate (Hz)	Over Sample Ratio	ADC Rate (Hz)	Current Est μA	Noise Est μT rms
0	0	0	0	0	80.00	16	1280	900.0	0.4
0	0	0	0	1	40.00	32	1280	900.0	0.35
0	0	0	1	0	20.00	64	1280	900.0	0.3
0	0	0	1	1	10.00	128	1280	900.0	0.25
0	0	1	0	0	40.00	16	640	550.0	0.4
0	0	1	0	1	20.00	32	640	550.0	0.35
0	0	1	1	0	10.00	64	640	550.0	0.3
0	0	1	1	1	5.00	128	640	550.0	0.25
0	1	0	0	0	20.00	16	320	275.0	0.4
0	1	0	0	1	10.00	32	320	275.0	0.35
0	1	0	1	0	5.00	64	320	275.0	0.3
0	1	0	1	1	2.50	128	320	275.0	0.25
0	1	1	0	0	10.00	16	160	137.5	0.4
0	1	1	0	1	5.00	32	160	137.5	0.35
0	1	1	1	0	2.50	64	160	137.5	0.3
0	1	1	1	1	1.25	128	160	137.5	0.25
1	0	0	0	0	5.00	16	80	68.8	0.4
1	0	0	0	1	2.50	32	80	68.8	0.35
1	0	0	1	0	1.25	64	80	68.8	0.3
1	0	0	1	1	0.63	128	80	68.8	0.25
1	0	1	0	0	2.50	16	80	34.4	0.4
1	0	1	0	1	1.25	32	80	34.4	0.35
1	0	1	1	0	0.63	64	80	34.4	0.3
1	0	1	1	1	0.31	128	80	34.4	0.25
1	1	0	0	0	1.25	16	80	17.2	0.4
1	1	0	0	1	0.63	32	80	17.2	0.35
1	1	0	1	0	0.31	64	80	17.2	0.3
1	1	0	1	1	0.16	128	80	17.2	0.25
1	1	1	0	0	0.63	16	80	8.6	0.4
1	1	1	0	1	0.31	32	80	8.6	0.35
1	1	1	1	0	0.16	64	80	8.6	0.3
1	1	1	1	1	0.08	128	80	8.6	0.25

5.5.2 CTRL_REG2 (0x11)

Table 31. CTRL_REG2 Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUTO_MRST_EN	—	RAW	Mag_RST	—	—	—	—

Table 32. CTRL_REG2 Description

AUTO_MRST_EN	Automatic Magnetic Sensor Reset. Default value: 0. 0: Automatic magnetic sensor resets off. 1: Automatic magnetic sensor resets on. Similar to Mag_RST, however, the resets occur before each data acquisition. This bit should normally be explicitly enabled by the user. This a WRITE ONLY bit and always reads back as 0.
RAW	Data output correction. Default value: 0. 0: Normal mode: data values are corrected by the user offset register values. 1: Raw mode: data values are not corrected by the user offset register values. **Note:** The factory calibration is always applied to the measured data stored in registers 0x01 to 0x06 irrespective of the setting of the RAW bit.
Mag_RST	Magnetic Sensor Reset. Default value: 0. 0: Reset cycle not active. 1: Reset cycle initiate or Reset cycle busy/active. When asserted, initiates a magnetic sensor reset cycle that will restore correct operation after exposure to an excessive magnetic field which exceeds the Full Scale Range (see Table 2) but is less than the Maximum Applied Magnetic Field (see Table 3). When the cycle is finished, value returns to 0.

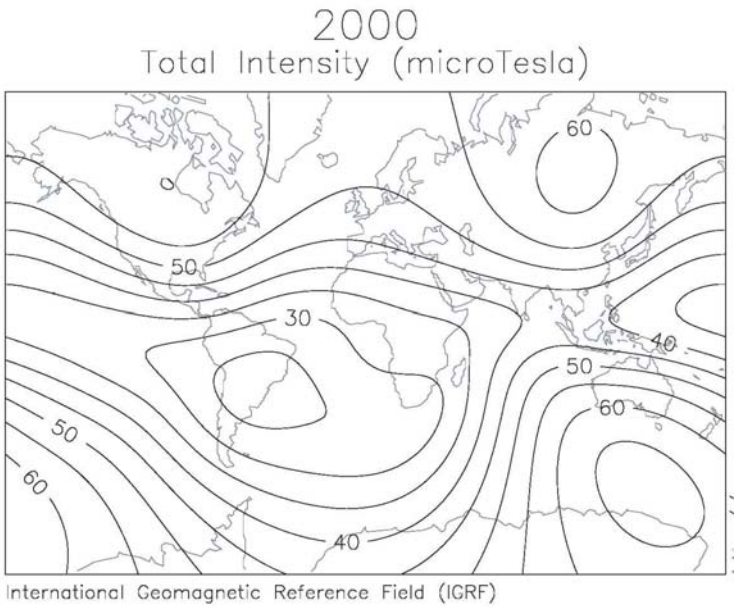
6 Geomagnetic Field Maps

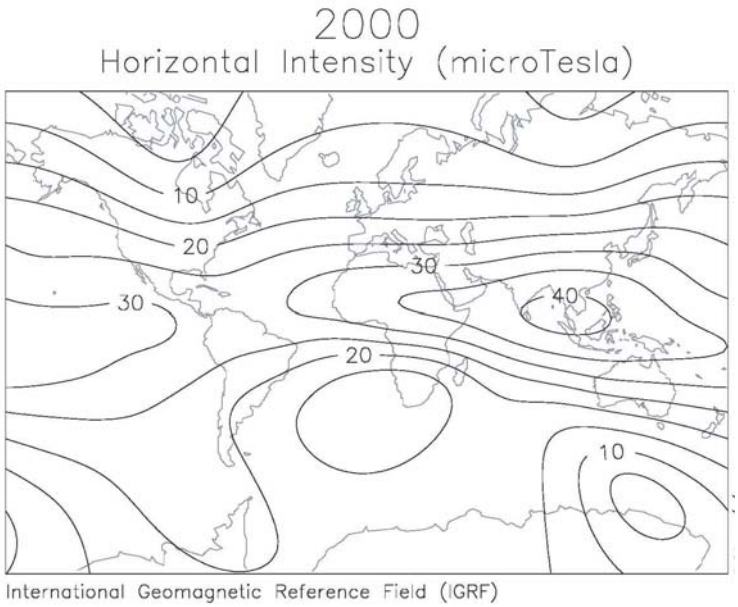
The magnitude of the geomagnetic field varies from 25 μT in South America to about 60 μT over Northern China. The horizontal component of the field varies from zero at the magnetic poles to 40 μT.

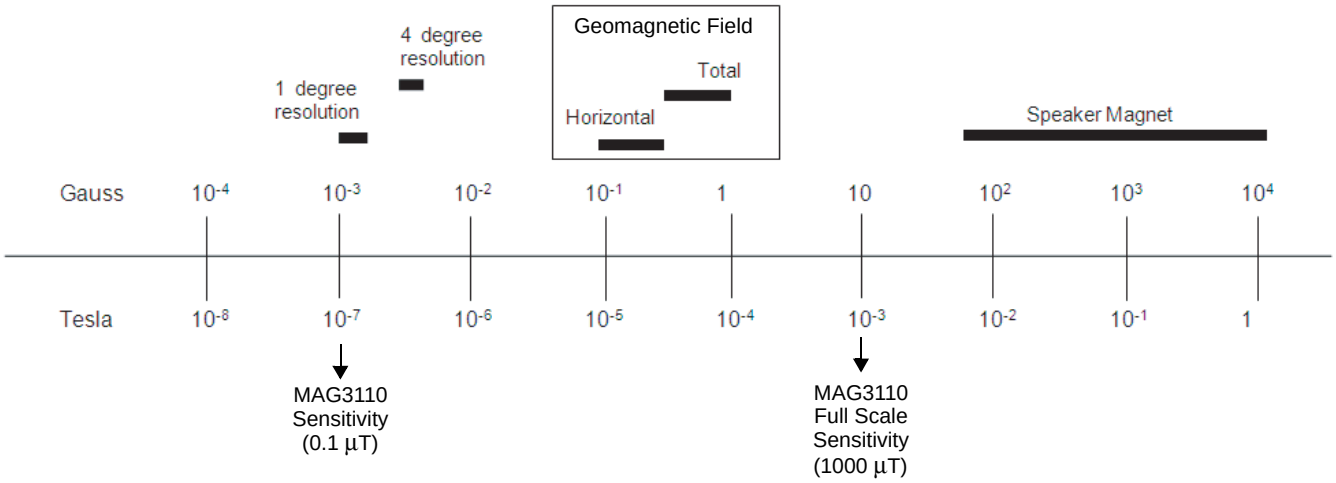
These web sites have further information:

http://wdc.kugi.kyoto-u.ac.jp/igrf/

http://geomag.usgs.gov






Geomagnetic Field
Total
Horizontal
4 degree resolution
1 degree resolution
Speaker Magnet
Gauss
10^{-4}
10^{-3}
10^{-2}
10^{-1}
1
10
10^{2}
10^{3}
10^{4}
Tesla
10^{-8}
10^{-7}
10^{-6}
10^{-5}
10^{-4}
10^{-3}
10^{-2}
10^{-1}
1
MAG3110 Sensitivity (0.1 µT)
MAG3110 Full Scale Sensitivity (1000 µT)

7 PCB Guidelines

Surface mount Printed Circuit Board (PCB) layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the PCB and the package. With the correct footprint, the packages will self-align when subjected to a solder reflow process. These guidelines are for soldering and mounting the Dual Flat No-Lead (DFN) package inertial sensors to PCBs. The purpose is to minimize the stress on the package after board mounting. The MAG3110 digital output magnetometers use the DFN package platform. This section describes suggested methods of soldering these devices to the PCB for consumer applications.

Please see Freescale application note AN4247,"Layout Recommendation for PCBs Using a magnetometer Sensor" for a technical discussion on hard and soft iron magnetic interference and general guidelines on layout and component selection applicable to any PCB using a magnetometer sensor.

Freescale application note AN1902, "Quad Flat Pack No-Lead (QFN) Micro Dual Flat Pack No-Lead (μDFN)" discusses the DFN package used by the MAG3110, PCB design guidelines for using DFN packages and temperature profiles for reflow soldering.

7.1 Overview of Soldering Considerations

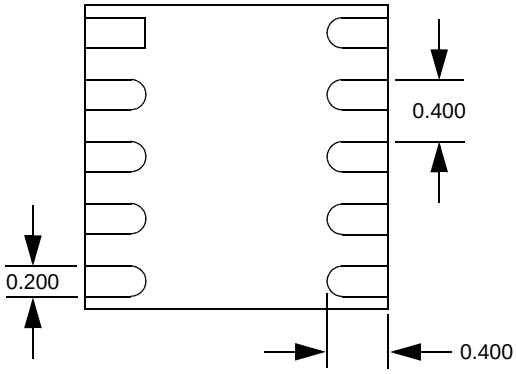
Information provided here is based on experiments executed on DFN devices. They do not represent exact conditions present at a customer site. Hence, information herein should be used as guidance only and process and design optimizations are recommended to develop an application specific solution. It should be noted that with the proper PCB footprint and solder stencil designs, the package will self-align during the solder reflow process.

7.2 Halogen Content

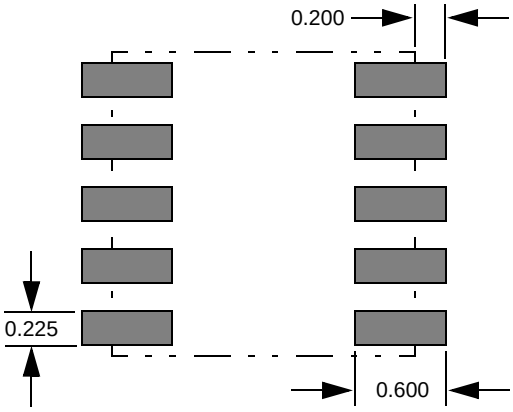
This package is designed to be Halogen Free, exceeding most industry and customer standards. Halogen Free means that no homogeneous material within the assembly package shall contain chlorine (Cl) in excess of 700 ppm or 0.07% weight/weight or bromine (Br) in excess of 900 ppm or 0.09% weight/weight.

7.3 PCB Mounting Recommendations

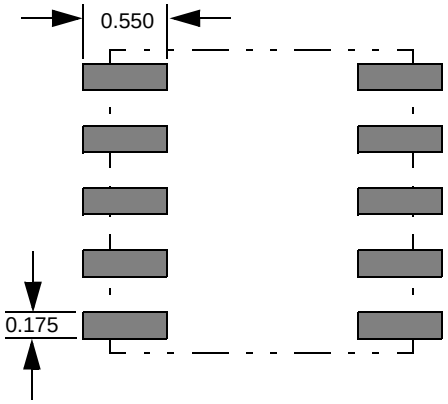
1. The PCB land should be designed as Non Solder Mask Defined (NSMD) as shown in Figure 7.
2. No additional via pattern underneath package.
3. PCB land pad is 0.6 mm by 0.225 mm as shown in Figure 7.
4. Solder mask opening = PCB land pad edge + 0.125 mm larger all around = 0.725 mm by 1.950 mm
5. Stencil opening = PCB land pad -0.05 mm smaller all around = 0.55 mm by 0.175 mm.
6. Stencil thickness is 100 or 125 mm.
7. Do not place any components or vias at a distance less than 2 mm from the package land area. This may cause additional package stress if it is too close to the package land area.
8. Signal traces connected to pads are as symmetric as possible. Put dummy traces on NC pads in order to have same length of exposed trace for all pads.
9. Use a standard pick and place process and equipment. Do not use a hand soldering process.
10. Assemble PCB when in an enclosure. Using caution, determine the position of screw down holes and any press fit. It is important that the assembled PCB remain flat after assembly to keep electronic operation of the device optimal.
11. The PCB should be rated for the multiple lead-free reflow condition with max 260°C temperature.
12. No copper traces on top layer of PCB under the package. This will cause planarity issues with board mount. Freescale DFN sensors are compliant with Restrictions on Hazardous Substances (RoHS), having halide free molding compound (green) and lead-free terminations. These terminations are compatible with tin-lead (Sn-Pb) as well as tin-silver-copper (Sn-Ag-Cu) solder paste soldering processes. Reflow profiles applicable to those processes can be used successfully for soldering the devices.



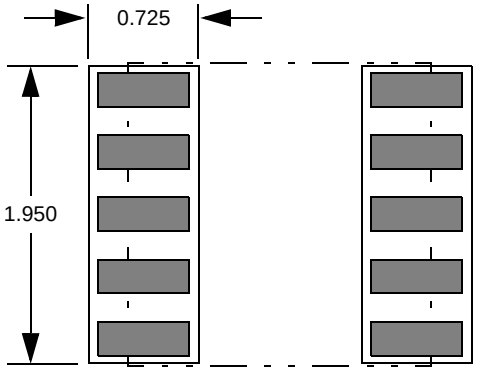
Package Footprint



PCB Cu Footprint



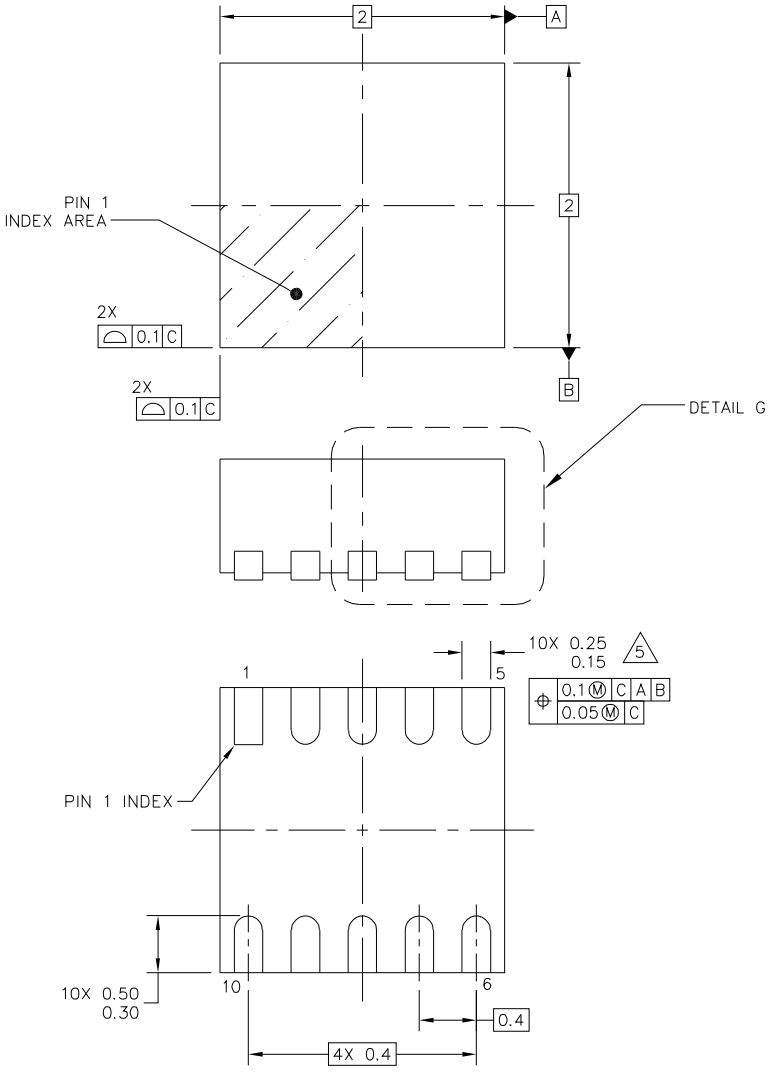
Stencil Opening



Solder Mask Opening

Figure 7. Footprints and Soldering Masks (dimensions in mm)

PACKAGE DIMENSIONS



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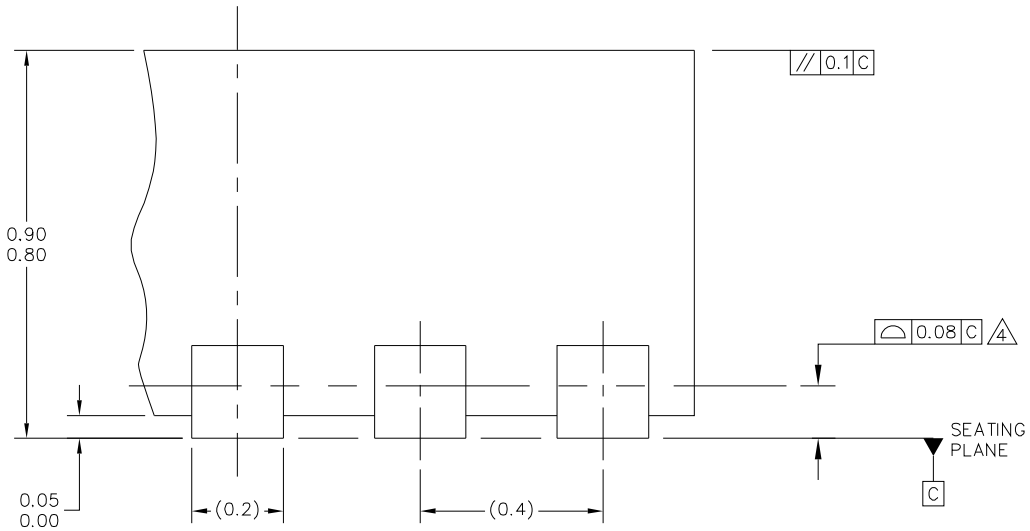
	CASE NUMBER: 2154–01	19 APR 2011
	STANDARD: NON–JEDEC	

CASE 2154-01
ISSUE O
10-PIN DFN

PACKAGE DIMENSIONS



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	STANDARD: NON–JEDEC	

CASE 2154-01
ISSUE O
10-PIN DFN

PACKAGE DIMENSIONS

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS IS NON JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO THE TERMINALS AND ALL OTHER BOTTOM SURFACE METALLIZATION.
5. THIS DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURE BETWEEN 0.15 AND 0.25 FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THIS DIMENSION SHALL NOT BE MEASURED IN THE RADIUS AREA.

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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
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China
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Fax: +1-303-675-2150
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